

- 1           1.    A method comprising:  
2                   forming a damascene via to a conductive line in  
3   the periphery of a phase change memory.
- 1           2.    The method of claim 1 including forming a phase  
2   change memory including a phase change storage element and  
3   a phase change threshold switch.
- 1           3.    The method of claim 2 including forming said  
2   switch over said element.
- 1           4.    The method of claim 3 including forming a pore  
2   over a substrate, said pore having a dimension smaller than  
3   the feature size possible with available lithographic  
4   techniques.
- 1           5.    The method of claim 4 including forming said pore  
2   by forming an aperture through an insulator and forming a  
3   sidewall spacer in said aperture.
- 1           6.    The method of claim 5 including forming the lower  
2   electrode of said phase change storage element in said  
3   pore.

1           7.    The method of claim 2 including forming a barrier  
2 layer between said threshold switch and said storage  
3 element.

1           8.    The method of claim 1 including forming an upper  
2 electrode that has a vertical extent at least twice its  
3 horizontal extent.

1           9.    The method of claim 2 including forming an upper  
2 electrode over said phase change storage element and said  
3 threshold switch, said electrode having sidewall spacers.

1           10.   The method of claim 9 including using said  
2 sidewall spacers as a mask to etch through underlying  
3 layers.

1           11.   The method of claim 1 including forming a  
2 plurality of cells as a plurality of integrated islands  
3 spaced from one another.

1           12.   The method of claim 11 including filling the  
2 regions surrounding said islands with an insulator.

1           13.   The method of claim 12 including forming said  
2 insulator to a height over the upper extent of said upper  
3 electrodes.

1        14. The method of claim 13 including forming grooves  
2 through said insulator down to and past the upper extent of  
3 said upper electrodes.

1        15. The method of claim 13 including forming a  
2 vertical groove in a memory array and a periphery.

1        16. The method of claim 15 including filling said  
2 groove in said periphery with a sacrificial light absorbing  
3 material.

1        17. The method of claim 16 including etching said  
2 groove in said periphery into said sacrificial light  
3 absorbing material.

1        18. The method of claim 17 wherein forming a  
2 damascene via includes filling said grooves with a  
3 conductive material.

1        19. The method of claim 18 including forming said  
2 groove in said periphery deeper than said grooves in the  
3 memory array.

1        20. The method of claim 19 including forming said  
2 grooves in said periphery to a depth below the upper extent  
3 of said upper electrode and above the lower extent of said  
4 upper electrode.

1        21. An apparatus comprising:  
2            a phase change material;  
3            a conductive line coupled to said phase change  
4 material; and  
5            a damascene via to said conductive line.

1        22. The memory of claim 21 wherein said memory  
2 includes a phase change storage element and a phase change  
3 threshold switch.

1        23. The memory of claim 22 wherein said switch is  
2 formed over said element.

1        24. The memory of claim 23 including a substrate, a  
2 pore over said substrate, said pore having a dimension  
3 smaller than the feature size possible with available  
4 lithographic techniques.

1        25. The memory of claim 24 including an insulator  
2 over said substrate, said pore formed as an aperture in  
3 said insulator, said pore having a sidewall spacer in said  
4 aperture.

1        26. The memory of claim 25 including an electrode for  
2 said phase change storage element in said pore.

1        27. The memory of claim 22 including a barrier layer  
2 between said threshold switch and said storage element.

1        28. The memory of claim 21 including an upper  
2 electrode having a vertical extent at least twice its  
3 horizontal extent.

1        29. The memory of claim 21 wherein said damascene via  
2 includes a metal line extending through an insulator.

1        30. A system comprising:  
2            a controller;  
3            a wireless interface coupled to said processor-  
4 based device; and  
5            a memory coupled to said device, said memory  
6 including a phase change material, a conductive line  
7 coupled to said phase change material, and a damascene via  
8 to said conductive line.

1           31. The system of claim 30 wherein said memory  
2 includes a phase change storage element and a phase change  
3 threshold switch.

1           32. The system of claim 31 wherein said switch is  
2 formed over said element.

1           33. The system of claim 32 including a substrate,  
2 said pore over said substrate, said pore having a dimension  
3 smaller than the feature size possible with available  
4 lithographic techniques.

1           34. The system of claim 33 including an insulator  
2 over said substrate, said pore formed as an aperture in  
3 said insulator, said pore having a sidewall spacer in said  
4 aperture.

1           35. The system of claim 34 including an electrode for  
2 said phase change storage element in said pore.

1           36. The system of claim 30 wherein said wireless  
2 interface includes a dipole antenna.